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JAZiO: Slow Edges Can Run Fast

A Novel Approach to High-Performance Bus Interfaces

By Kevin Krewell {2/21/00-02}

To understand what JAZiO is and how it performs, put aside everything you know, or think you know, about interface design. Clear your mind of ground bounce, fast slew rates, ringing, clock jitter, setup times, and hold times. Put traditional synchronous logic design out of your head. And—as Monty Python would say—now for something completely different.

JAZiO promises the ability to transfer very high speed digital data with slower edge-rate signals than was possible before and with noise margins comparable to true differential signals. JAZiO's answer to fast bus design changes the ground rules by not judging a logic state purely in the voltage domain on a fixed clock edge. Instead, JAZiO determines the data by detecting a change, or the absence of a change, from the preceding state over a full bit time. Differential sensing in the interface design allows better noise margins at lower voltage swings. JAZiO mixes several innovative ideas, each of which can be broken out as a separate idea but which together provide the robust characteristics required of a high-speed system bus.

Bus Topology and Signaling

The layout of a JAZiO bus would typically be composed of up to 18 data lines and two complementary control signals: VTR (voltage-time reference) and VTR#. The VTR signals provide both a reference voltage and a clock (actually a bit time reference) for the data signals as each data line is compared simultaneously with both true and complement VTR lines. The 18 data and two VTR signals are routed in a bundle to achieve a common-mode-noise component in both data and VTR signals. Power-supply noise and ground bounce at the drivers also appear as common-mode noise on the data signals and VTR signals and this noise is subtracted by the differential comparators, increasing system noise margins.

In order to achieve differential sensing, each data signal uses dual comparators to compare the data signal with both VTR signals. Since the two VTR signals are complementary, it follows that one of them is the complement of the data—the comparator with the *greater* difference is used to supply the internal data bit. This dynamic selection process, coupled with close routing of the data and VTR signals, achieves common-mode-noise rejection almost as efficiently as true

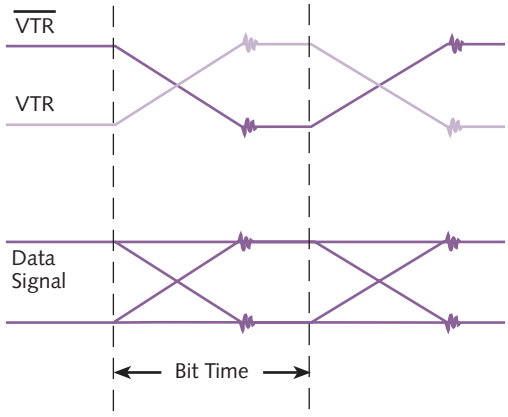

Figure 1. A bit time is shown in this simplified timing waveform. Common-mode noise induced on a data signal and VTR signals will be subtracted by the appropriate differential receiver.

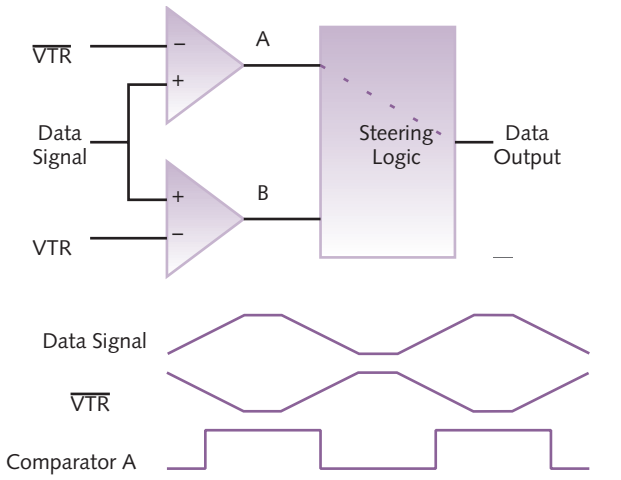

Figure 2. The input data signal is compared against both VTR and its complement. The switching logic selects the correct comparator. An example data waveform is shown against the VTR# signal, forming a differential signal output from comparator A.

differential signaling, and it is substantially better than pseudo-differential inputs that use a static reference voltage.

The signal comparison occurs during the time that the VTR signal is transitioning from one level (e.g., low) to the opposite level (e.g., high), as Figure 1 shows. The interface does not require setup or hold times and utilizes the full bit time to determine the bit state. A bit time is defined as the period that the VTR signal transitions from one level to the other (high-to-low or low-to-high). In effect, if you consider VTR as a clocking signal, it allows data to be transferred on both "edges" of VTR. Synchronization of the received data is then left to the system designer to implement, allowing systems to utilize a global clock or to use different clocking domains, possibly using a clock recovered from the complementary VTR signals.

During each bit time, a decision must be made as to which VTR signal provides the larger differential. The choice of the appropriate comparator is made by the steering logic shown in Figure 2. The steering logic required to make the selection is quite simple, as Figure 3 shows. Part of the steering logic generates true and complement select lines (SL and SL#) from the VTR lines. The output state and select lines are compared using XOR gates to determine which comparator will be used for the next state. If, from bit time to bit time, the data input changes state, the same comparator is selected; if the data remains unchanged, the steering logic toggles the comparator selection. In this manner, the data output line always has the benefit of the comparator with the greater signal difference.

Figure 4 shows an example data transfer. The bus is initialized by holding a high or "1" state on the data input prior to starting the VTR signals. A low or "0" state is represented by the transition from high to low in time step 1. At this time, comparator A is selected and the data appears on the output after a delay of less than one bit time. In time step 2, the input changes to a "1" and the output of comparator A continues to provide a rail-to-rail output. At time step 3, the input bit remains a "1" and comparator A begins to drop out of its saturation state as the difference between the input signal and VTR diminishes. At that time, the steering logic flips the switches to the strongly driven comparator B. The switch is glitchless because the outputs of both comparators are at the same ("1") state during the transition.

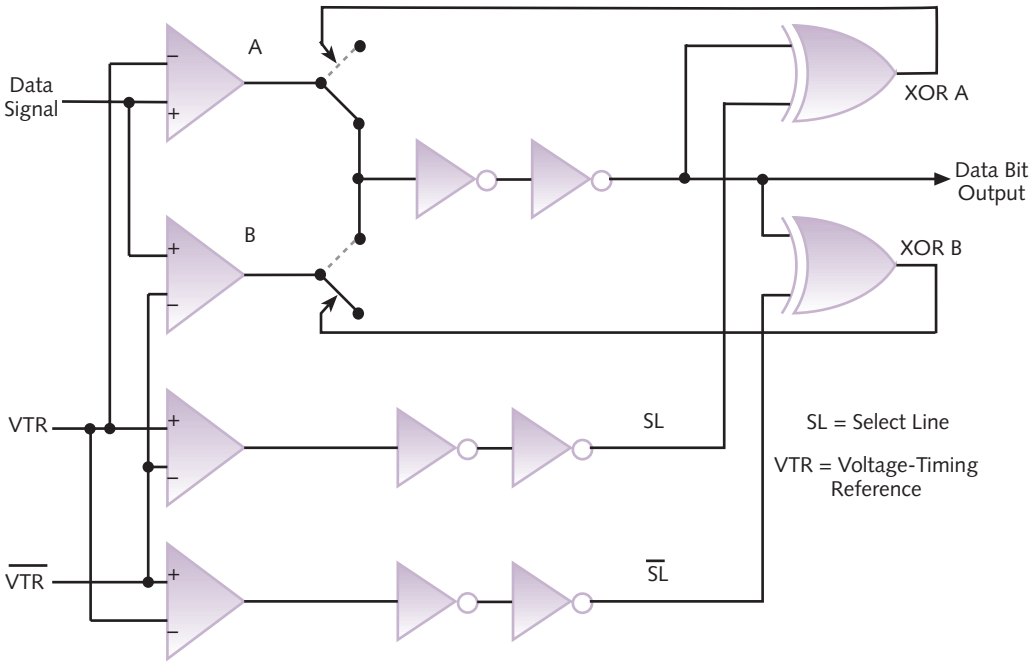

Figure 3. A more detailed look at the steering logic shows that it depends on a comparison between the output data state and the select lines (SL) to determine the correct comparator for the next data state. If data is switching, the XOR gate compares it against the changing SL signal and continues to select the same comparator. If the data does not change state in the early part of the bit time, the XOR gates toggle the selection of the comparator.

System Benefits

The trend in interface signals today is toward ever-higher frequencies and ever-lower voltage swings. With this trend

come lower noise margins and higher channel bit error rates. Fast driver slew rates create problems such as transient voltage drops (bypass issues), ground bounce, and transmission line effects like ringing, overshoot, and undershoot. The JAZiO interface allows slower edge rates and provides better noise margins than single-ended signals without the expense (in pins) of traditional differential pairs. Figure 5 illustrates the advantages of JAZiO's slow slew rate and the noise-margin improvements resulting from the differential between VTR and the data input.

JAZiO's slower edge rates reduce EMI, simplify transmission line designs, and reduce instantaneous driver currents. But JAZiO is also suitable for low-power interface designs, because it doesn't require high-current drivers, and it can operate below 1.0 V and still provide better noise margins than single-ended designs.

Another advantage of low-voltage swings is that the interface can run at high frequencies without requiring extremely fast slew rates. The engineers at JAZiO have simulated the interface up to 1.6 GHz with a 200-ps signal skew, using 0.35-micron technology. The company says that even higher frequencies are distinctly possible using a more modern process technology. Additional robustness can be had with a programmable de-skewing circuitry in the I/O cell. Although JAZiO technology has not been realized in any system design today, it will be only a matter of time before the concept is demonstrated in a shipping product.

Reducing the number of signals and pins saves packaging costs, reduces EMI, and simplifies board layout. JAZiO also allows point-to-multipoint transmission lines, whereas other high-speed signaling solutions, such the EV6 bus and the AGP bus, achieve their speed by restricting signals to point-to-point links. The interface allows the VTR signals to be wire-ORed between multiple drivers with one cycle of dead time during a changeover. Because, JAZiO does not inherently require a phase-locked-loop (PLL) circuit, VTR signals can be stopped at any time and restarted, allowing the interface to exist in a static state when not in use.

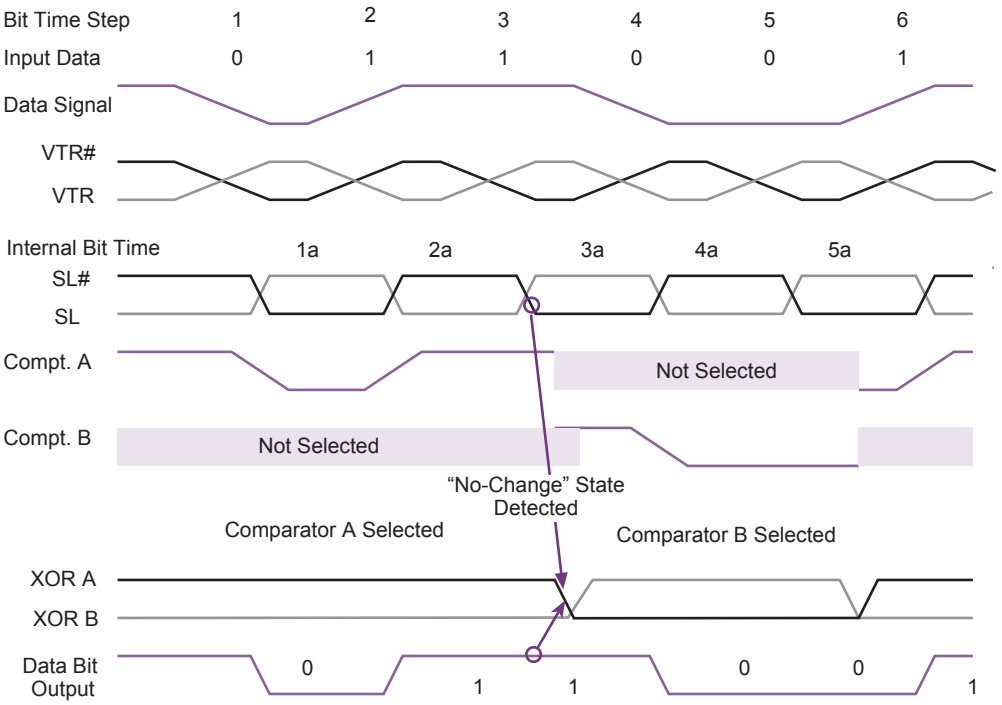

Figure 4. The example shown in Figure 3 demonstrates how the steering logic operates under various data conditions. In time steps 1 and 2, data is switching and the logic chooses comparator A to drive the data out. In time step 3, the data does not change from step 2, so the logic switches the comparators as comparator B provides the correct differential signal.

The Prospects for JAZiO

JAZiO is a small company that licenses technology IP for an innovative, high-performance interface design. Before you think, "Oh no, not another Rambus," understand that the

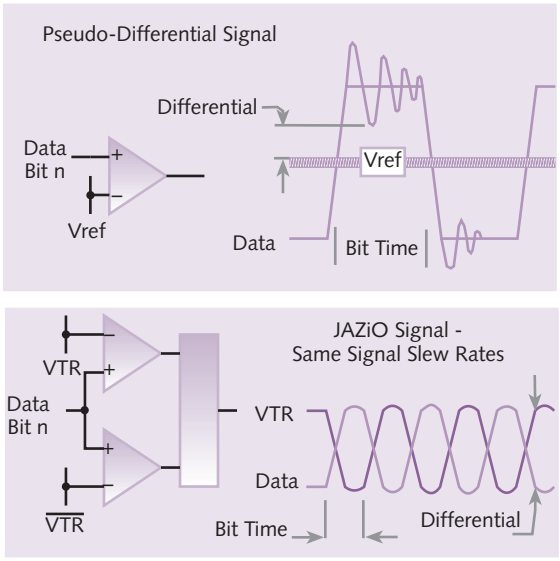

Figure 5. JAZiO differential signaling is compared with psuedo-differential signaling. Noise margin is increased and higher data throughput is achieved with the same slew rate. The noise margin can be traded off for lower signal levels, which can also help to lower signal slew rates.

engineers at JAZiO have taken the opposite business approach, and there are no grandiose schemes to corner the DRAM market. JAZiO consists of a small team of engineers who believe they have a better way to solve the problems contemporary high-performance system designers face, including noise, transmission line effects, the need for more bandwidth, and keeping costs reasonable. The JAZiO team filed for a number of patents and is offering the technology under conventional patent licensing terms. JAZiO is not attempting to create a new standard, but it would like to see the technology adopted by an existing standards body.

JAZiO will need a high-profile design or adoption by an open standards committee to push the technology into the mainstream of system interfaces. For Rambus, the Nintendo 64 design win gave it some momentum, but not until its endorsement by Intel for desktop computers did the Rambus technology became a candidate for mainstream acceptance.

Price & Availability

JAZiO license is available for $200,000 and 0.3% royalty for DRAM, which includes 100 hours of consulting services. For additional information contact JAZiO at 408.487.1810 or at *info@jazio.com*. Also you can see the Web site at *www.jazio.com*.

One of the beauties of JAZiO technology is that it is applicable to a wide range of interfaces, including buses for memory, processors, backplanes, communications, and graphics. It can also be used for internal chip buses. Considering the potential of JAZiO and the modest goals of its creators, the technology should find a home soon—perhaps even in that multi-gigahertz PC you'll have in a few years.