JAZiO™ Incorporated

JAZiO™ Business Development Model

- General purpose high performance inter-chip or intra-chip signaling technology, addressing markets where performance is the differenciator as compared to standards or infrastructure.
- Enabling intra-chip technology for system-on-chip & embedded memory.
- Low power and wide operating range (frequency and voltage), allows quick penetration into portable applications where standards are still evolving.
- Superior performance, frequency and power supply scalability will enable JAZiO™ to take over memory interface technology in a few years.

Digital Signaling Techniques

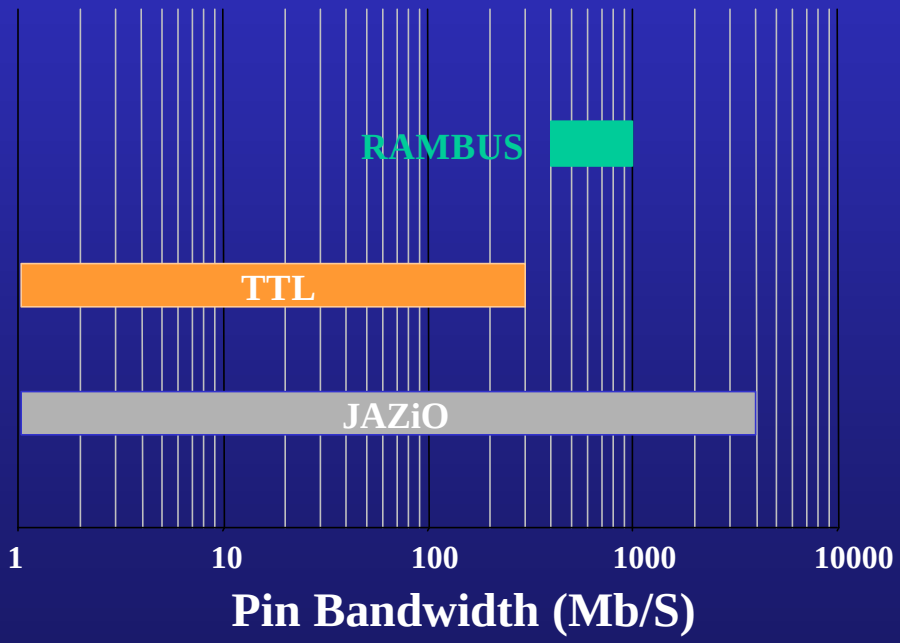
Differential	• (Ext. I/F): LVDS, RSDS, Gigablaze • (Int. I/F): Similar to SRAM • Very small swing, high speed, low power, but double the pins or signal lines
Psuedo Differential (One Fixed Reference)	• (Ext. I/F): GTL, HSTL, Rambus, SSTL • (Int. I/F): Similar to DRAM • Medium swing, medium speed, medium power
Single-Ended (Ratio Stage With Ground As Reference)	• (Ext. I/F): TTL, LVTTL, CMOS • (Int. I/F): Similar to Data and Address buses • Large swing, load dependent speed and power
JAZiO (‘Change’ or ‘No Change’ From Previous State)	• ……... • ……... • Small swing, high speed and low power for large interconnect dominated load

Technology Features

➢ CONCEPT	TOTALLY NEW
➢ SIMULATED PERFORMANCE	>1 GIGABITS/SEC/PIN
➢ DIE SIZE PENALTY	VERY SMALL TO NEGLIGABLE
➢ I/O POWER	< 50mW per I/O (1.8V Bus termination)
➢ PROTOCOL	VARIOUS
➢ LICENSE TERMS	UNRESTRICTED (Per Mkt Segment)
➢ RELIABILTY	ROBUST
➢ SCALABILITY	SCALABLE (to >2GigaBits/sec/pin)
➢ SIGNAL SWING	500mV single ended

I/O Interface Operating Range Comparison

JAZiO™ optimizes the pins, power, and bandwidth for any application.



I/O Interface Target Market Comparison

- No protocol restriction
- Easily scaleable with voltage and technology
- Higher integration

What Makes JAZiO™ Unique?

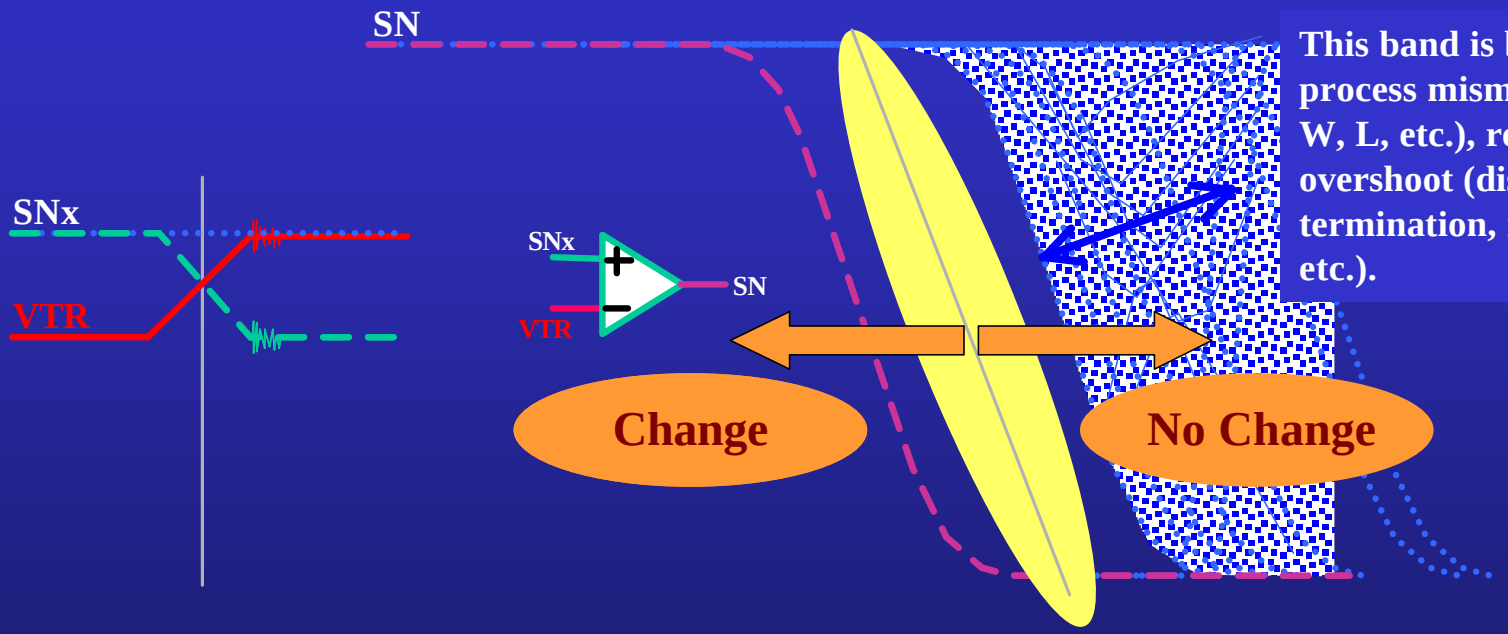
The major concept that makes the JAZiO™ single ended signaling unique is, the receiver detects “change” versus “no change”, while conventional receivers detect either “high level” or “low level” relative to a reference (“high current” or “low current” relative to a reference).

Input and Output Circuitry

The input and output circuitry can be subdivided into five sections to better understand the concepts individually before the complete interface is put together.

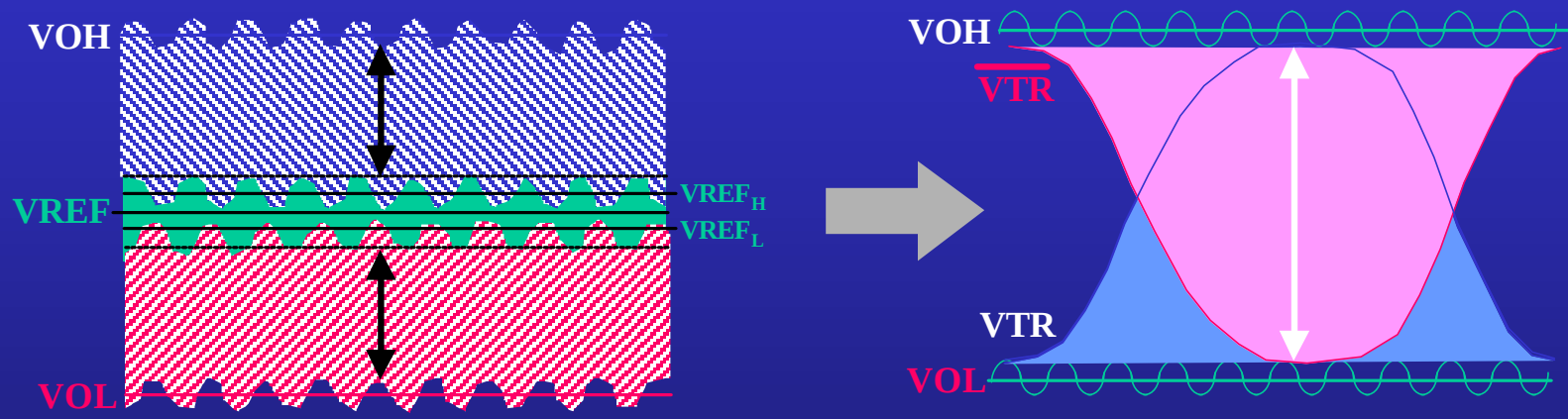
- Signal Change Discriminator
- Alternating References
- Dual Comparator
- Initialization
- Steering Logic

Signal Change Discriminator



- Quickly amplifying the signal if a logic change has occurred
- Some time gap compared to the signal logic change case followed by indeterminate voltage, when no logic change has occurred in the signal
- The time gap is dependent on signal swing, reference signal transition time, process mismatch and signal reflection, etc.

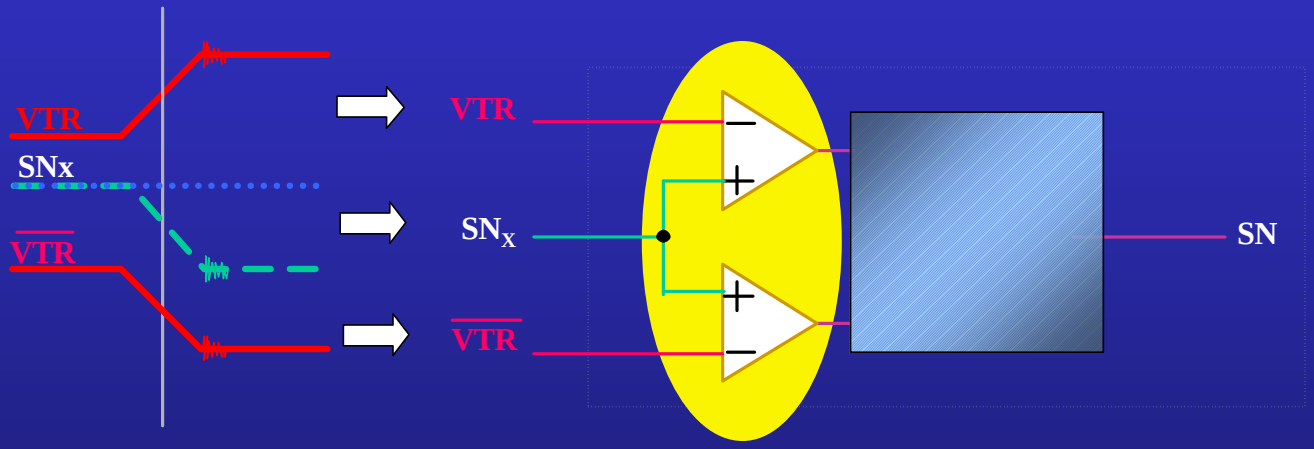
Alternating References



Changes VREF to VTR

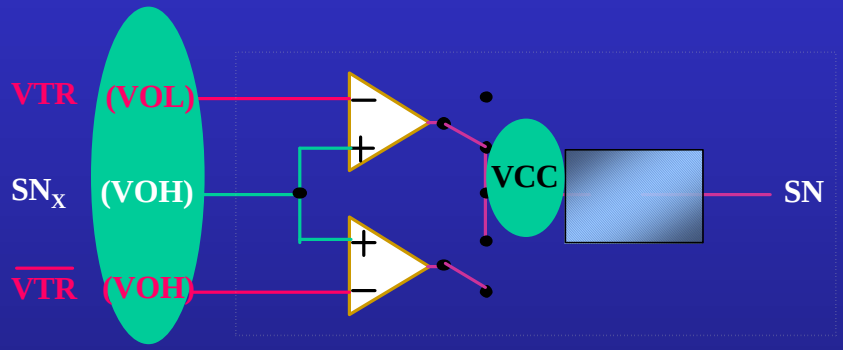
- Reduces VREF variation component of signal swing
- Larger differential signal when signal changes
- Removes a discrete level from the swings
- Reduces signal slew rate to achieve the same differential swing

Dual Comparator



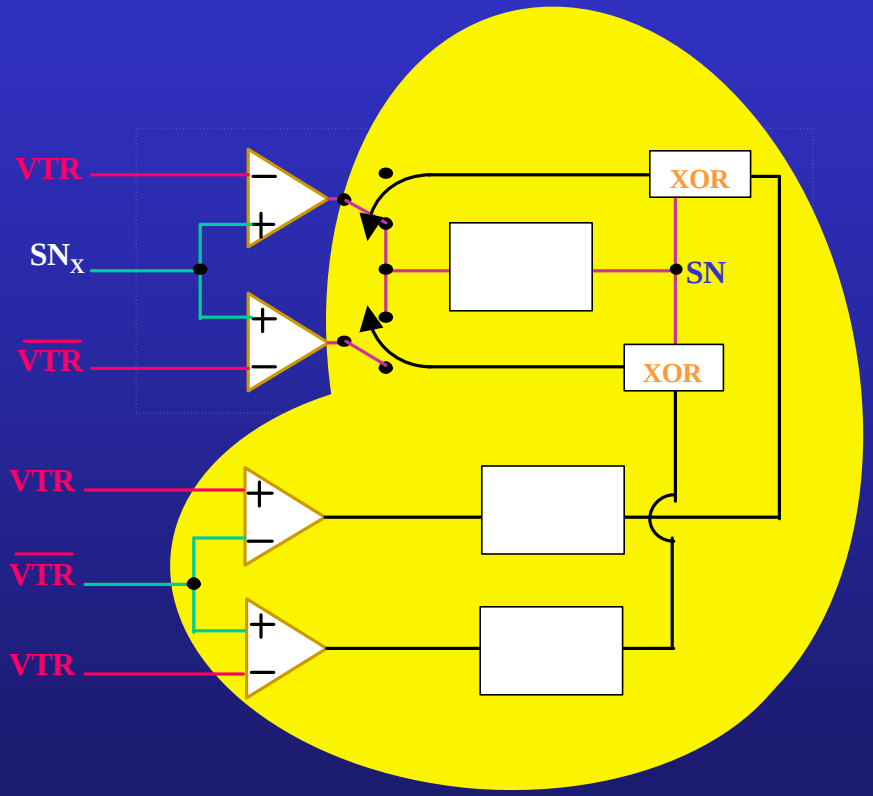
- Ready for the next signal change
- Maintains and restores signal actively when no signal changes

Initialization



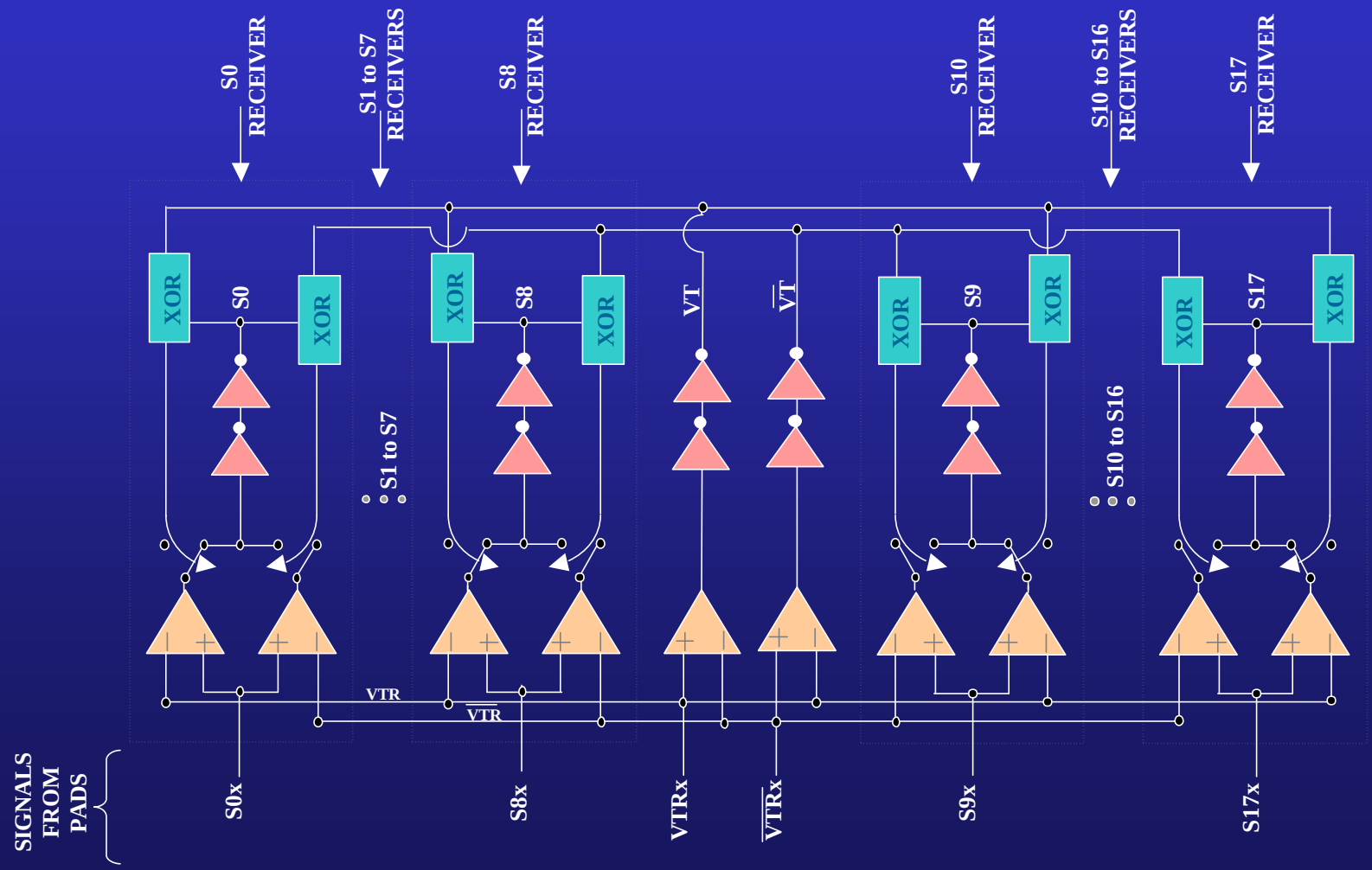
- Starting the receiver input and output at the same logic level to enable the steering logic properly
- Start with the higher voltage level on all signals to reduce power

Steering Logic

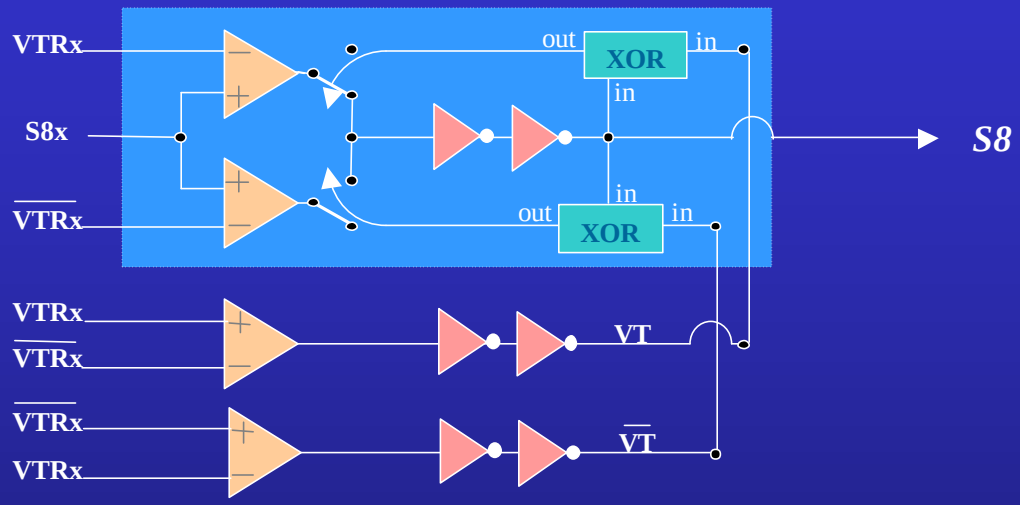


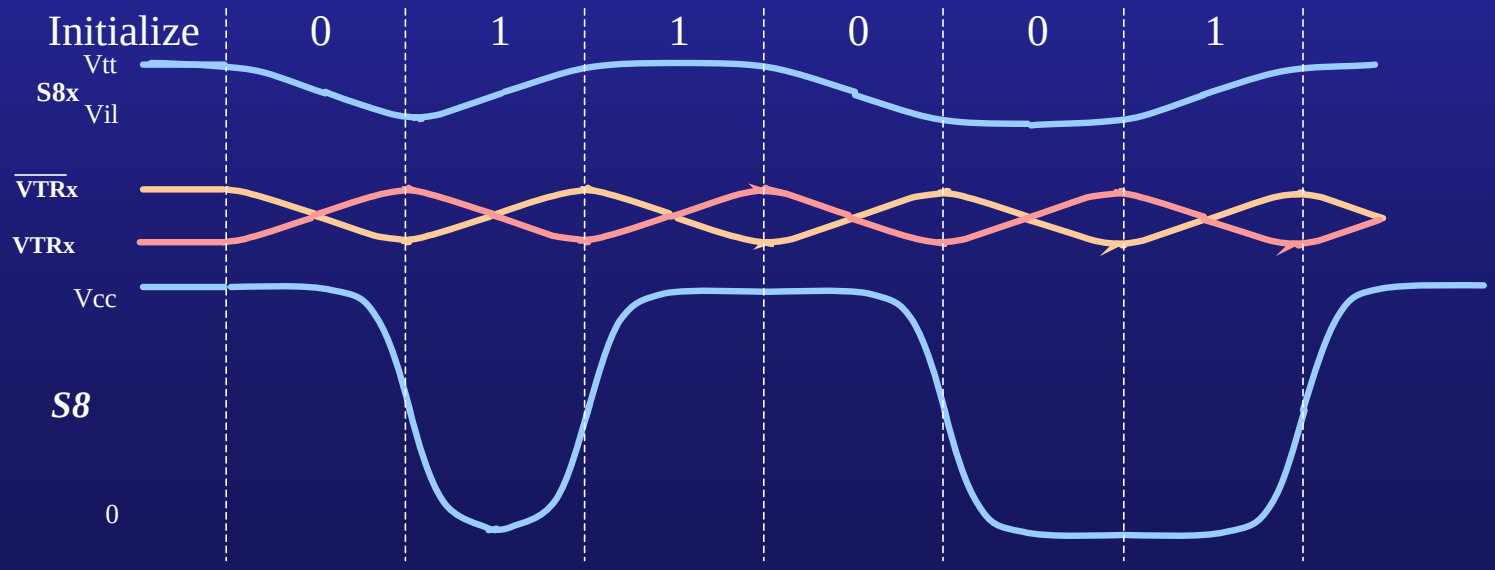
- Close the switch for the comparator with differential signal
- Maintain the switch if the signal changes
- Reverse the switch if no signal change

JAZiO™ Receiver



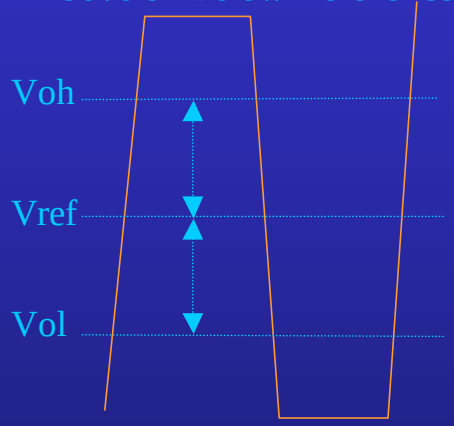
JAZiO™ Receiver Operation





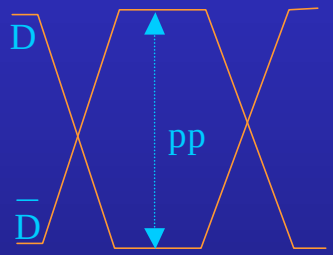
Voltage to Time Domain Transposition

Above or Below Reference



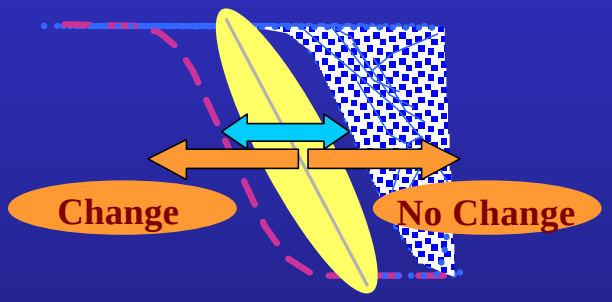
Psuedo-Differential
(SSTL, RSL, GTL, etc.)

Peak to Peak Difference



LVDS

Change vs No Change Gap

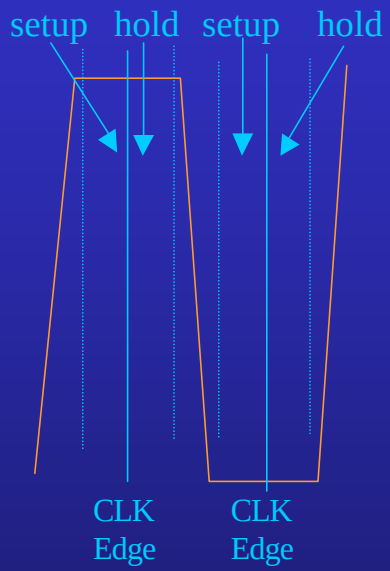


JAZiO

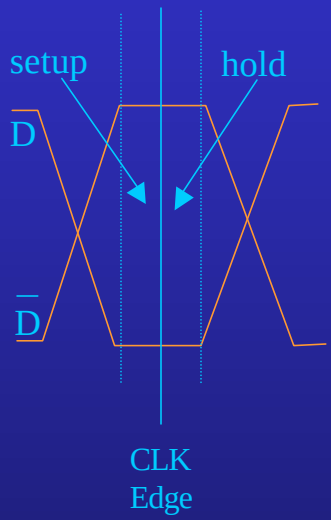
JAZiO transposes the voltage domain to the time domain, since signal binary is defined in the time domain.

JAZiO binary margin is more dependent on transition time rather than voltage swing.

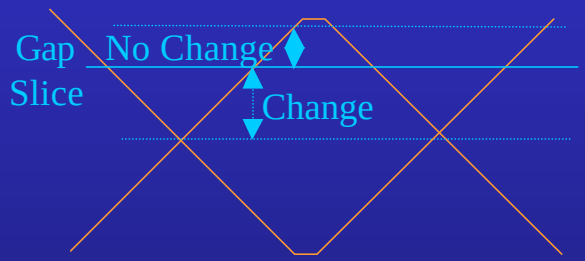
Design Margin



Psuedo-Differential
(SSTL, RSL, GTL, etc.)



LVDS



JAZiO

Fast signal transition time is better for setup and hold time margins in Psuedo-differential and differential.

Slow signal transition time is better for large gap between change and no change in JAZiO.

Logical Event Detection Reversal

Present Paradigm

Previous Data ⇨ High Z / Equalization ⇨ New Data

or

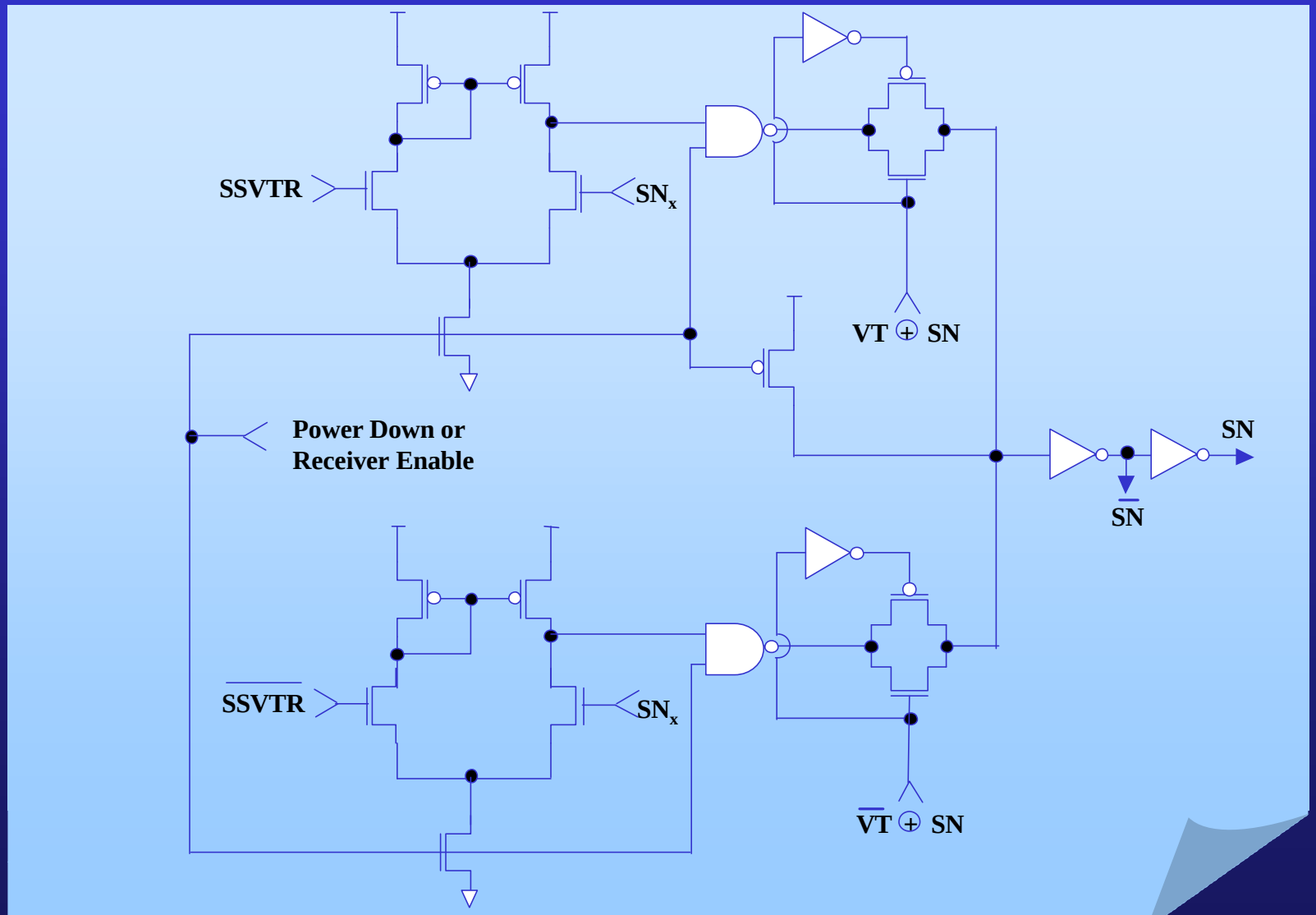
Previous Data ⇨ New Data

JAZiO Paradigm

Change ⇨ No Change

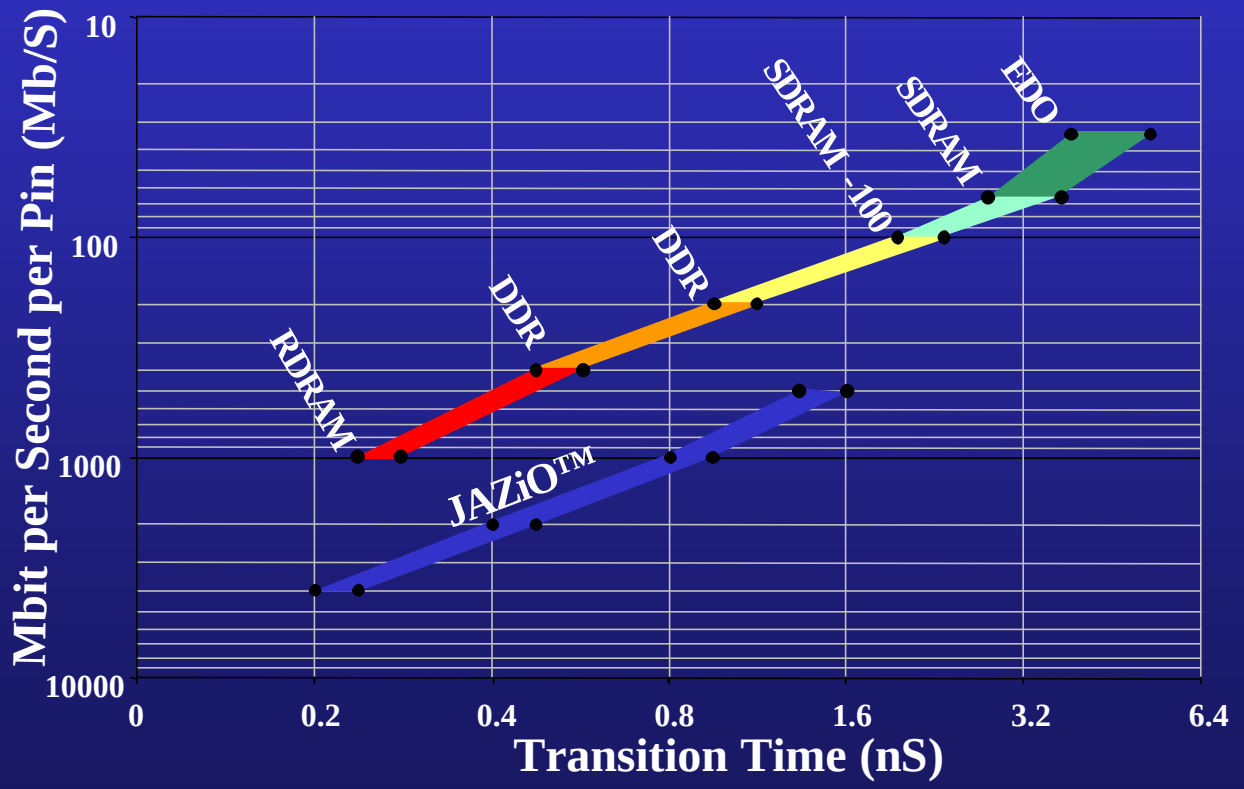
JAZiO paradigm looks for change to occur prior to the reference time.

Present paradigm compares the voltage levels on the inputs to the reference level.


SSVTR
SNx
VT ⊕ SN
Power Down or
Receiver Enable
SN
SN
SSVTR
SNx
VT ⊕ SN

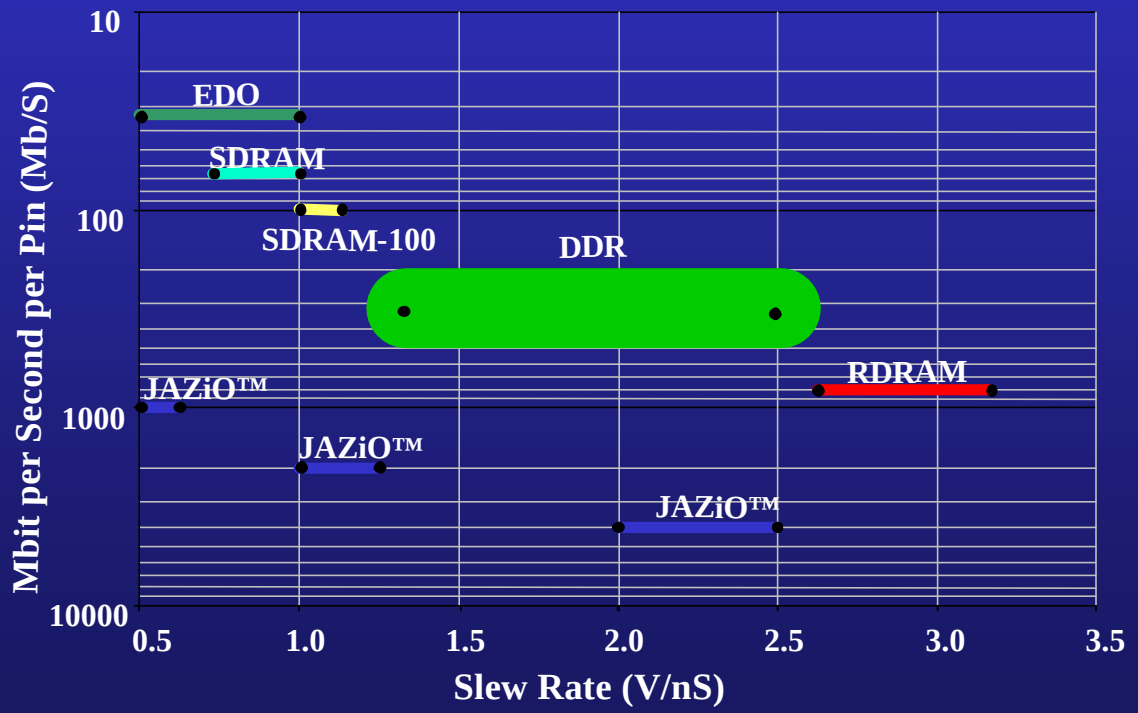
I/O Interface Transition Time Comparison

- Reduced noise
- Improved margins
- Improved scalability



I/O Interface Slew Rate Comparison

- Reduced edge current
- Reduced cross talk
- Higher reliability



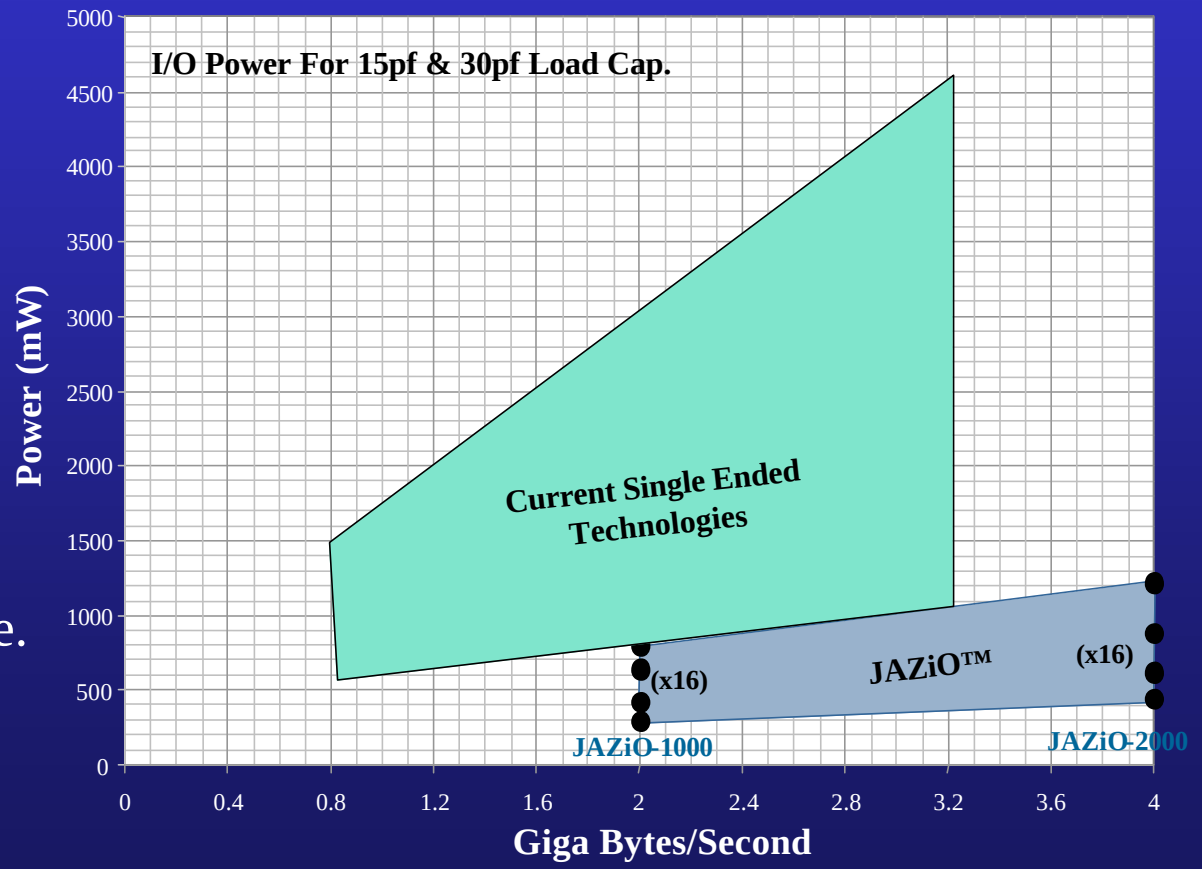
I/O Interface Power Comparison

The system can be optimized to achieve:

Cost reduced package and lower system cost

or

Higher integration: more pins for more performance.



Design Optimization

Step 1

Design DC bias point of the differential amplifier to be approximately (Voh+Vol)/2 (with typical conditions) with a gain of 3 to 4.

Step 2

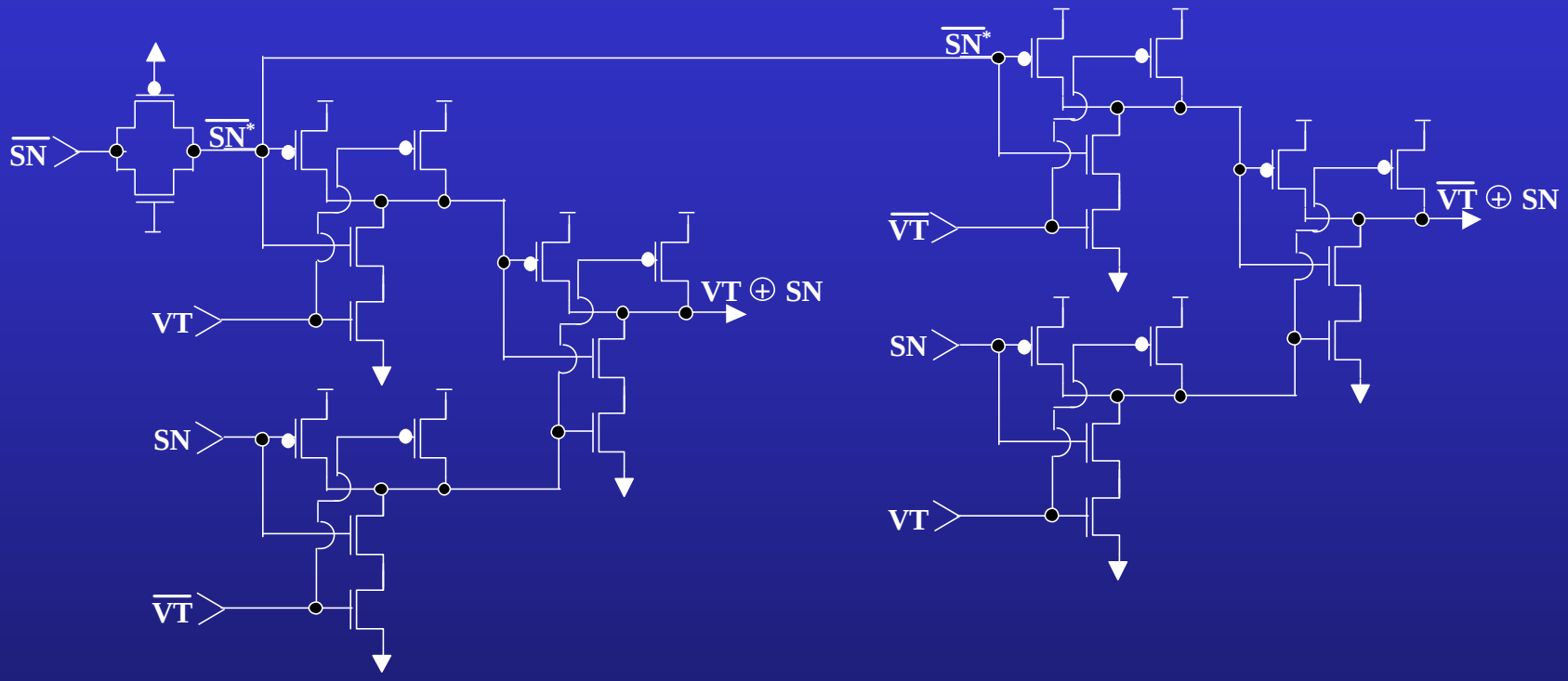
Line up $\overline{SN}$*, SN, $\overline{VT}$, VT to cross at the mid-point and look symmetrical to one other (with typical conditions).

Step 3

Design the XOR to have no glitches and to cross low with 200pS skew in the external SNx (with typical conditions).

Step 4

Design the output driver for slow turn-on and turn-off, to get symmetric rise and fall times and a transition time equal to 80% of the data rate (with typical conditions) up to a max of 2nS.

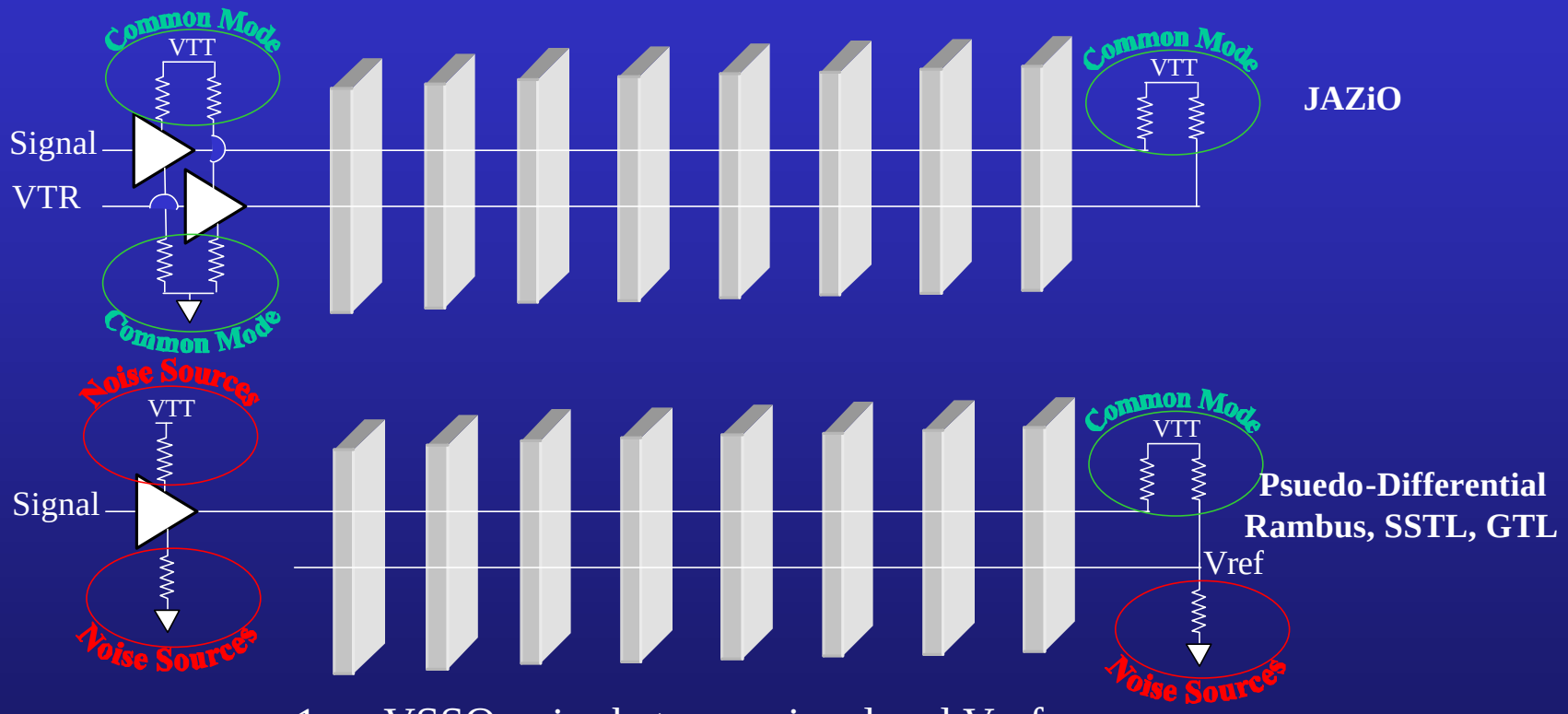


The XORs should act like a low-pass filter (slow path).
First stage nand gates bias point should be approximately mid-point.
Second stage nand gate bias point should be 1/3 to 1/4 VCC.

Noise Issues

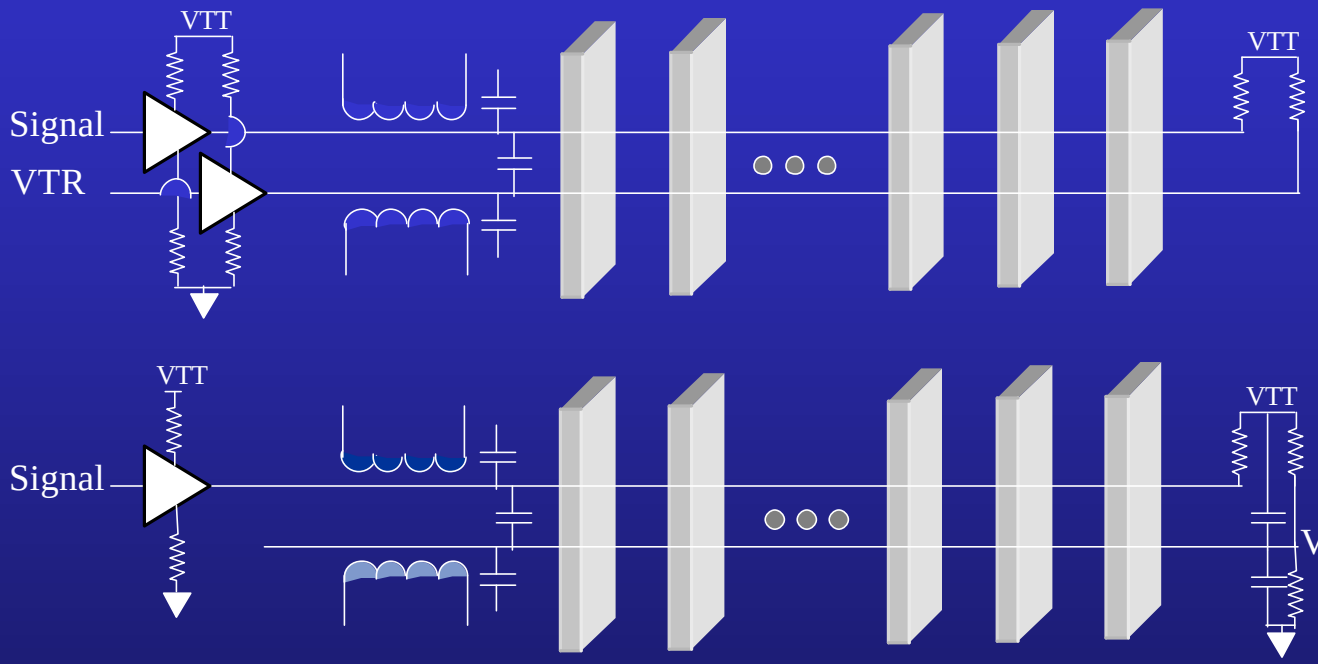
	JAZiO		Existing Single-Ended
	Change	**No Change**	
Power Supply (Vssq & Vtt)	More signal making it less susceptible.	Same impedance & bias conditions, making power supply noise common mode.	Different impedance & bias conditions makes the noise a big factor.
Signal Coupling or Cross talk	Slow transition reduces the cross talk considerably. Either impedes the reference(s)/signal(s) transition, or has no effect.	Slight variation but the low impedance & slower transition reduces the effect substantially.	Faster transition time for high frequency is a major contributor in reducing signal.
Reflections or Termination Noise	Slow transition time is useful in reducing the reflection, which is the most important noise in JAZiO.		Critically damped termination is absolutely essential for maximum frequency operation.

Power Supply Noise Issues



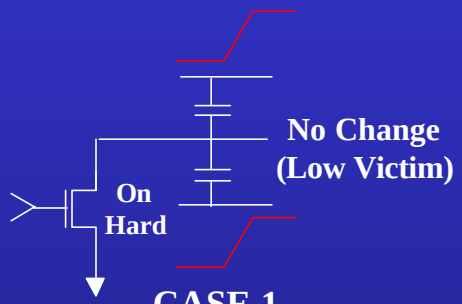
1. VSSQ noise between signal and Vref.
2. VTT noise and/or VTT mismatch on either end.
3. Vref impedance to Signal impedance mismatch.

Environmental Noise Issues

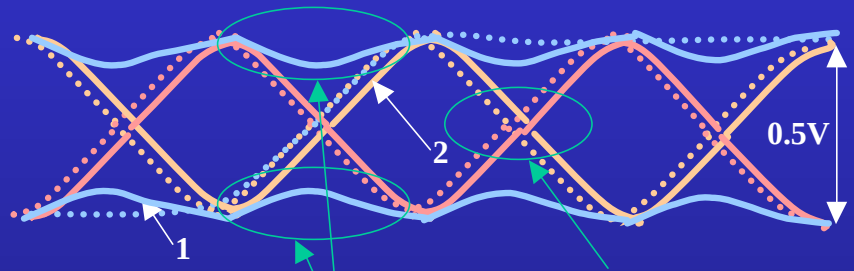


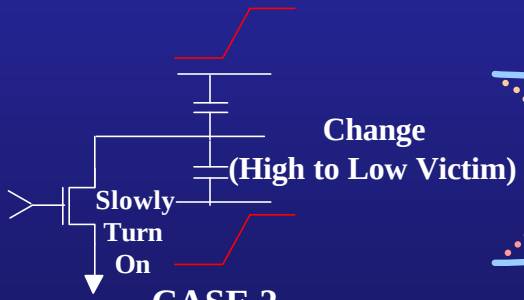
1. Slower transition generates less noise in JAZiO.
2. Smaller transition generates less noise in JAZiO.
3. VTR's are isolated by VSS to eliminate noise variations.
4. Board dimension has not shrunk as rapidly as on-chip dimensions.

Environmental Noise Issues

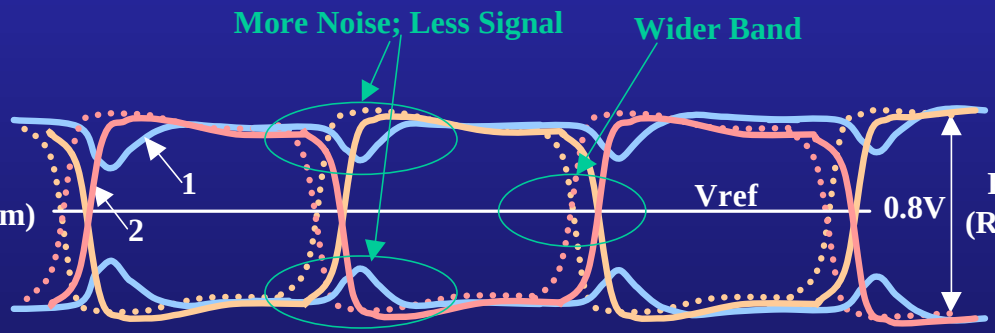


CASE 1



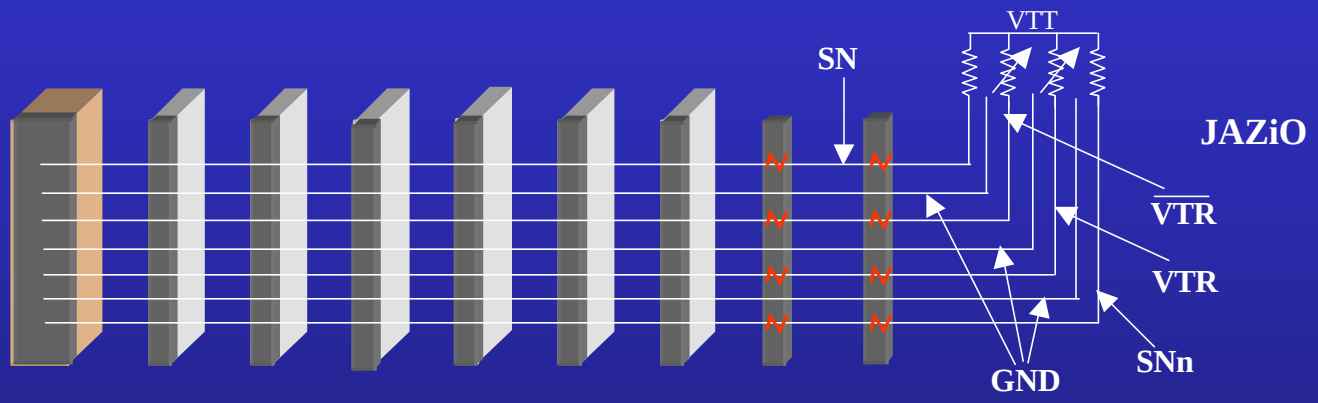


CASE 2



Noise (No Change)
Noise (Change)
No Noise (No Change)
No Noise (Change)

Reflections & Termination Issues

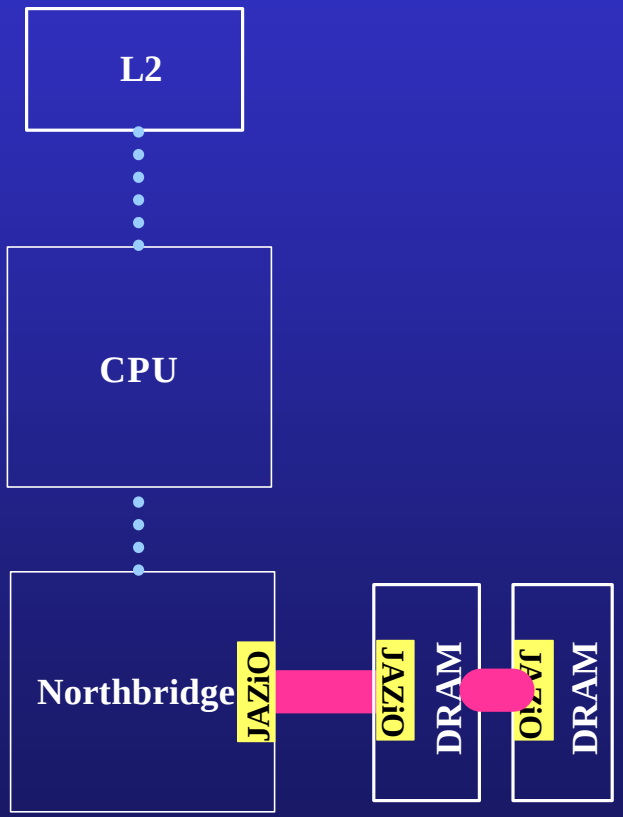


- VTR's need to be well terminated with as little overshoot/undershoot as possible.
- VTR's should be designed to be as monotonic as possible.
- The signals will have noise only when they change, but by having larger signal during the change the noise effect is less than other single-ended technologies.

Improvements over current single ended signaling

- Reduced signal swing ~0.5V
- Noise reduction & cancellation
- Power reduction
- Ease of implementation for inter-chip or intra-chip
- Scalability with Voltage
- Low area penalty
- Easily scalable for wider busses (x64 etc.)

DRAM Application Example



JAZiO can be used between Northbridge and DRAM to achieve even greater than 2 GBit/pin/sec bandwidth.

JAZiO's signaling technology allows bus expansion in both depth and width. No restriction on bus protocol or definition.

JAZiO is a low latency interface.

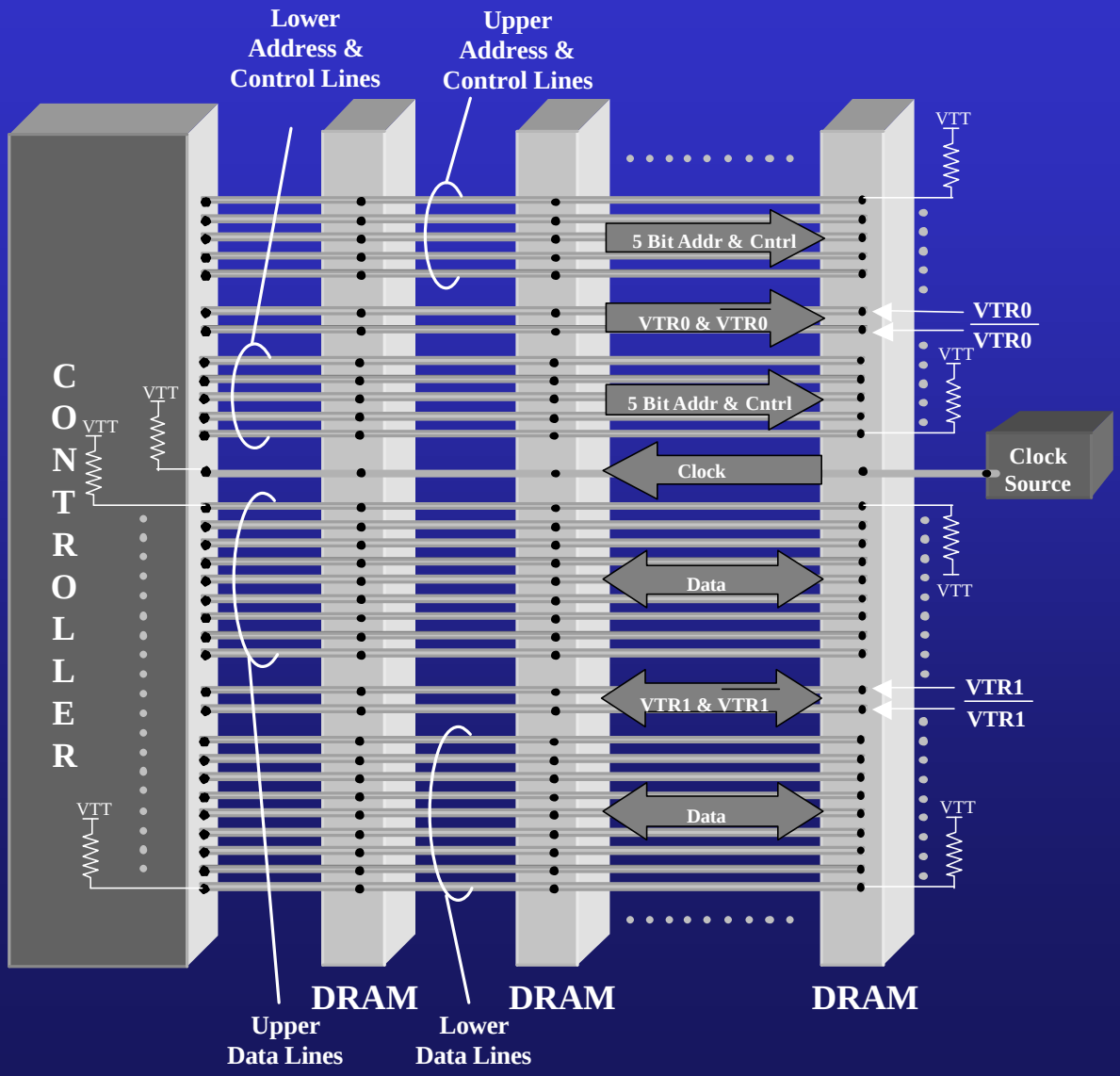
JAZiO makes implementation easier and takes the burden off of meeting set-up time, hold time, and rise/fall times. JAZiO requires no PLL or DLL circuitry to work..

Single cycle power-up initialization allows user to fully utilize standby/sleep mode.

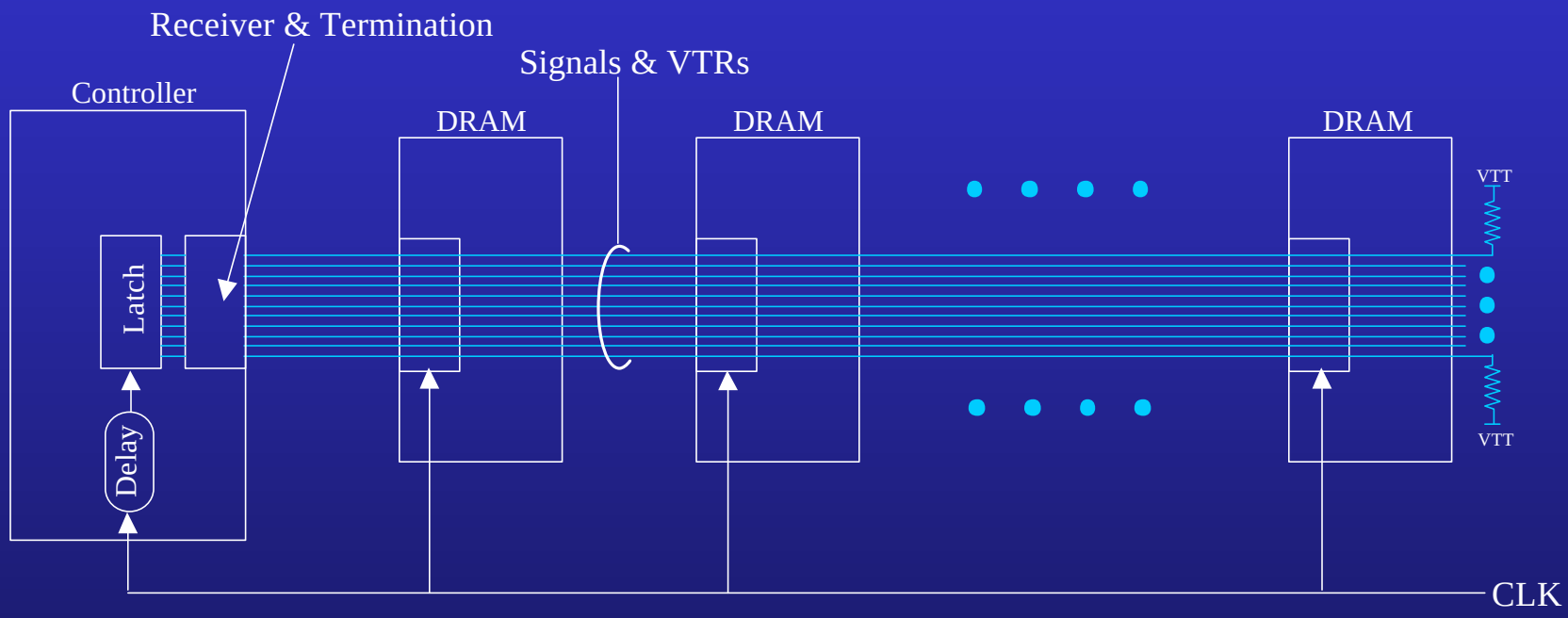
Low power and wide operating frequency improves DRAM cost.

JAZiO's small voltage swing and slow transition time allows multiple slots with terminations at both ends. Easily adaptable for large memory systems (like servers).

Better performance and scalability compared to Rambus and SSTL.

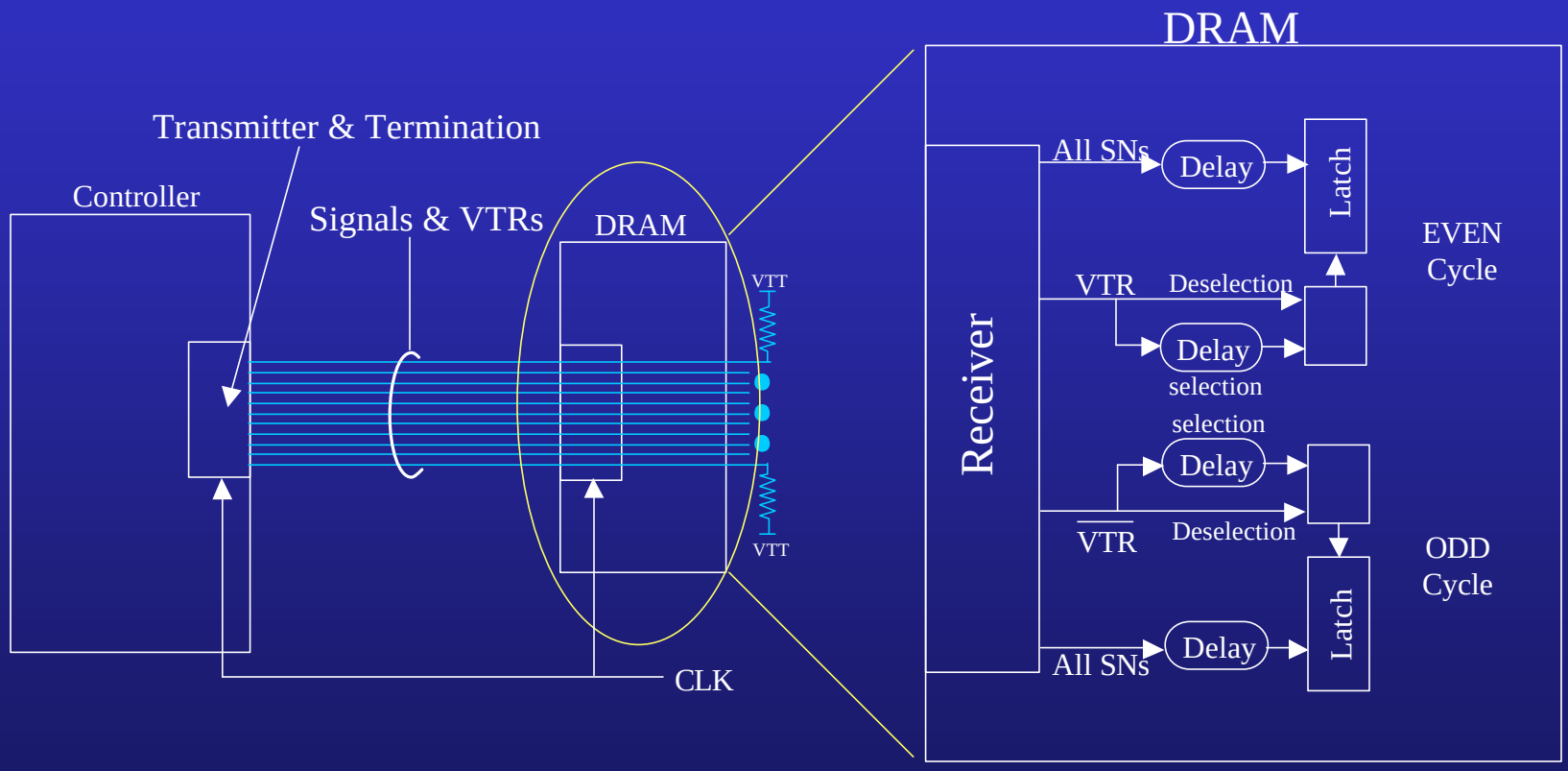

Lower
Address &
Control Lines
Upper
Address &
Control Lines
CONTROLLER
VTT
VTT
VTT
VTT
VTT
VTT
VTT
5 Bit Addr & Cntrl
VTR0 & VTR0
5 Bit Addr & Cntrl
Clock
Data
VTR1 & VTR1
Data
VTR0
VTR0
VTR1
VTR1
Clock
Source
DRAM
DRAM
DRAM
Upper
Data Lines
Lower
Data Lines

Data Flow From DRAM To Controller



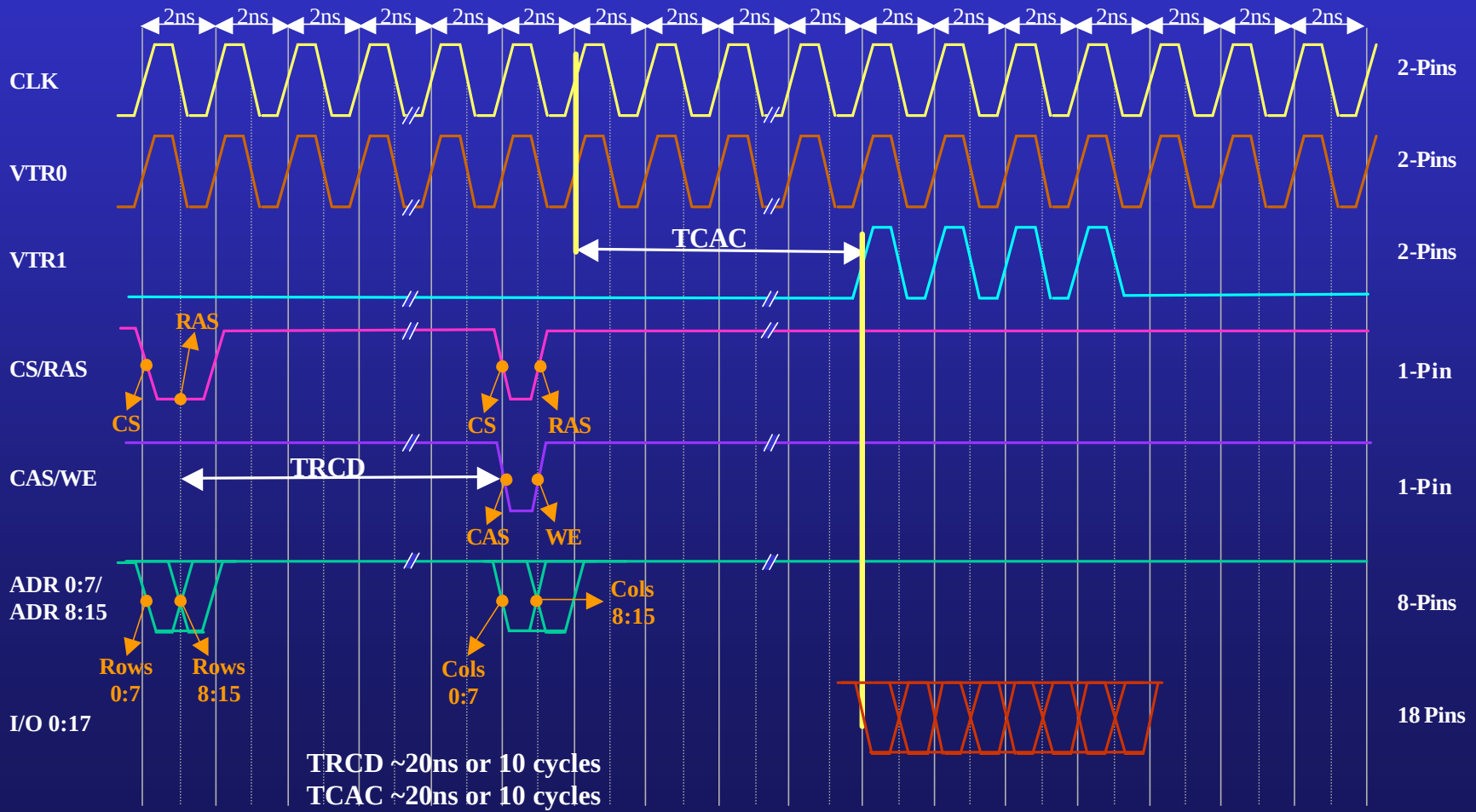
Data and VTRs arrive at the controller at the same time, independent of the DRAM which is sending the data.

Data Flow From Controller To DRAM

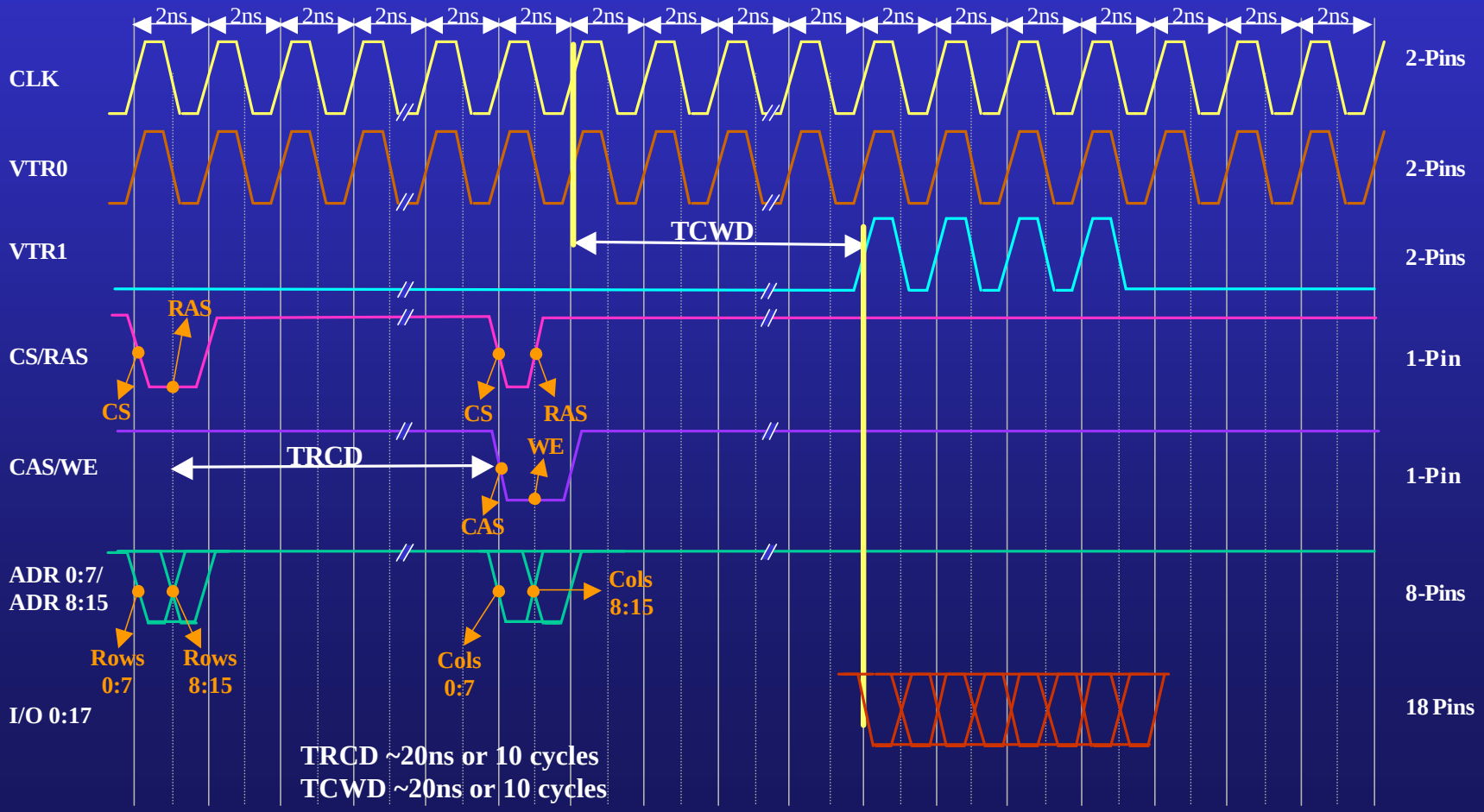


SN delay can be used for pre-decoding of addresses or logical selection with control signals. VTR and $\overline{\text{VTR}}$ are used for latching signals (SNs).

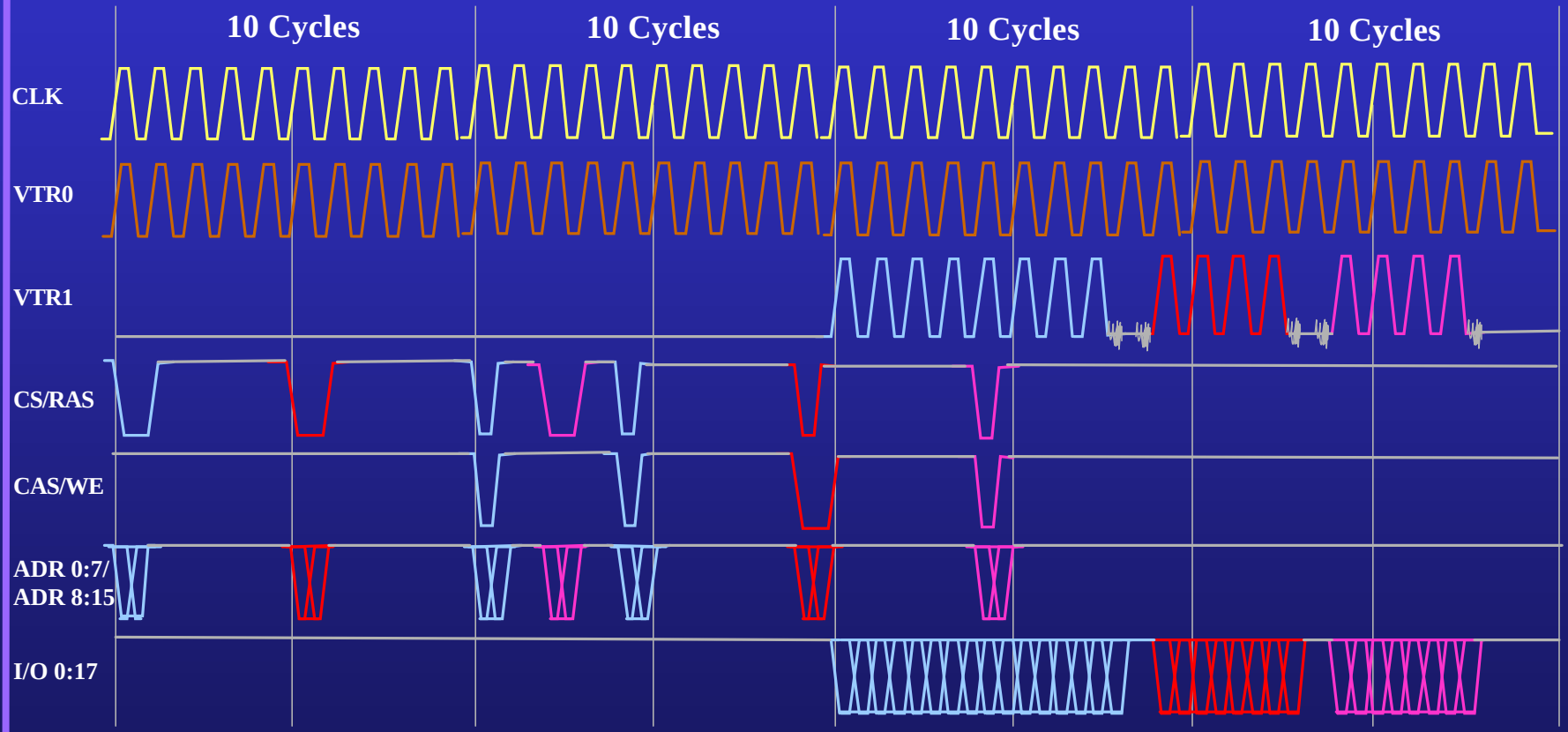
Read Cycle 8-Bit Burst

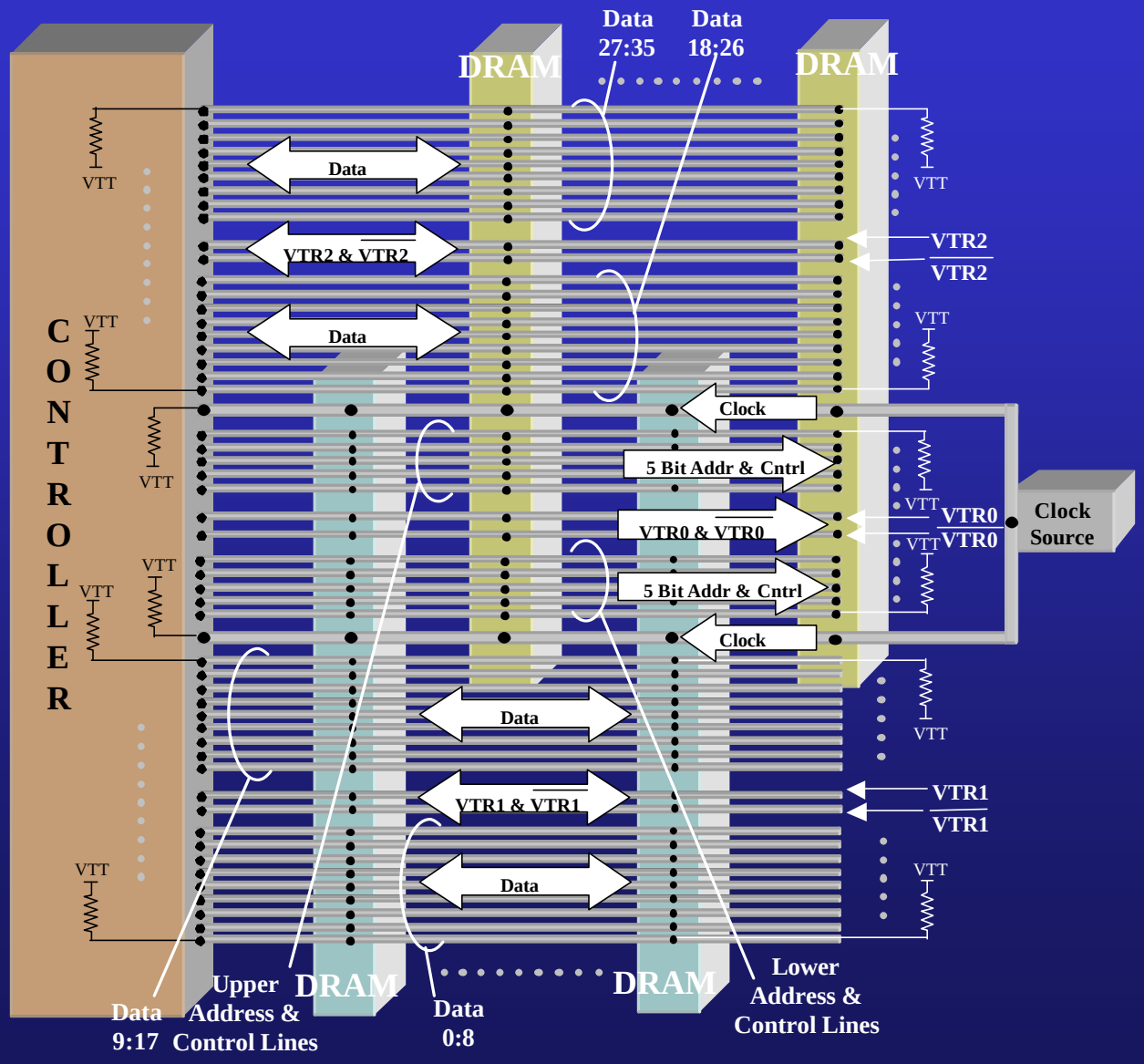


Write Cycle 8-Bit Burst

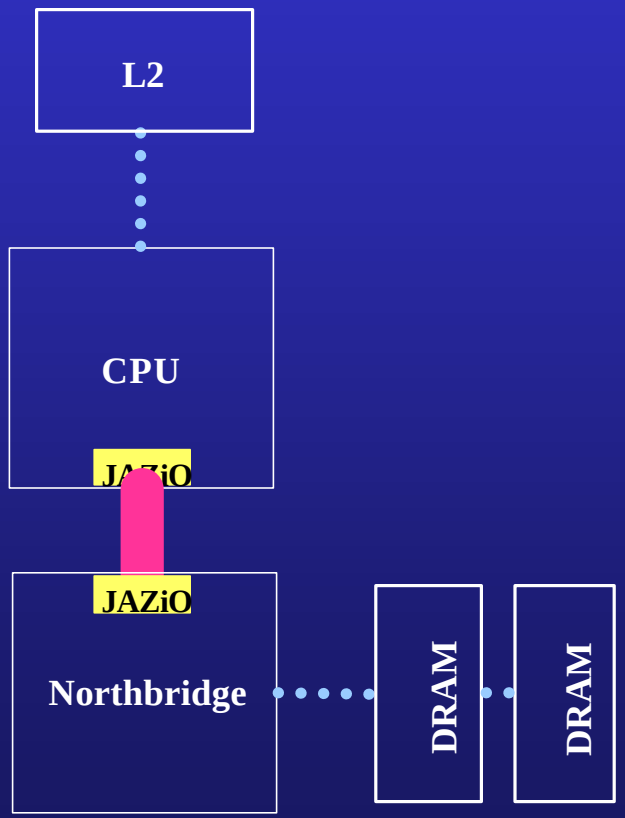


Read, Read,Write, Read Burst




DRAM
DRAM
Data 27:35
Data 18:26
CONTROLLER
VTT
Data
VTR2 & VTR2
VTR2
VTR2
Clock
5 Bit Addr & Cntrl
VTR0 & VTR0
VTR0
VTR0
Clock Source
5 Bit Addr & Cntrl
Clock
Data
VTR1 & VTR1
VTR1
VTR1
Data
DRAM
DRAM
Data 9:17
Upper Address & Control Lines
Data 0:8
Lower Address & Control Lines

CPU to Controller Application Example



JAZiO can be used in a proprietary bus between CPU and the Northbridge to achieve even greater than 10 GBytes/sec bandwidth.

JAZiO bus can essentially run at the same frequency as the internal CPU clock.

No restriction and full differentiation on bus protocol and definition.

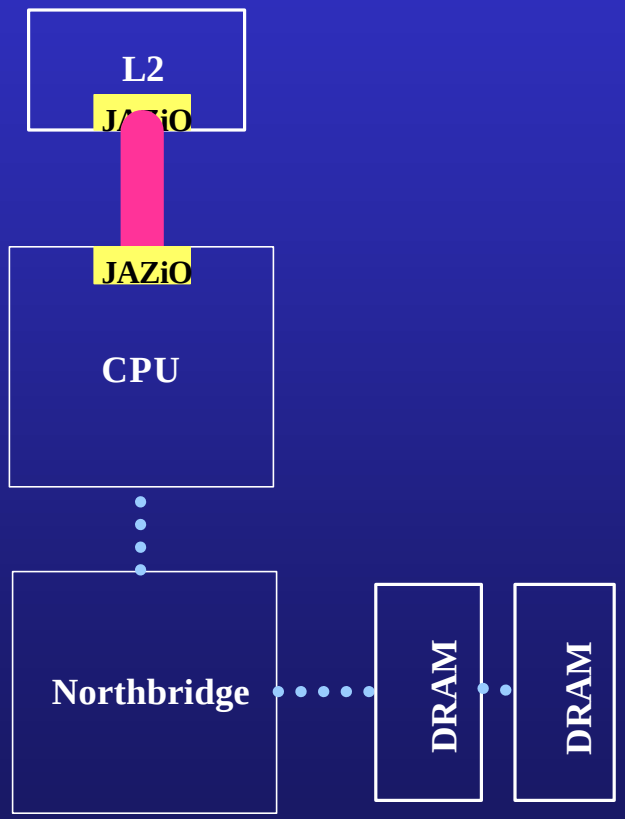
Lower pin count and power as a result of single-ended giga hertz per pin signaling technology.

Single cycle power-up initialization allows user to fully utilize standby/sleep mode.

Lower cost in packaging and heat sink requirements due to reduced pins and power.

Better performance and scalability compared to GTL+ and HSTL.

CPU to SRAM Application Example



JAZiO can be used between CPU and SRAM (L2) to achieve even greater than 2 GBit/pin/sec bandwidth.

JAZiO bus can essentially run at the same frequency as the internal CPU clock.

Low latency interface.

Easily adaptable to support multiple cache sizes.

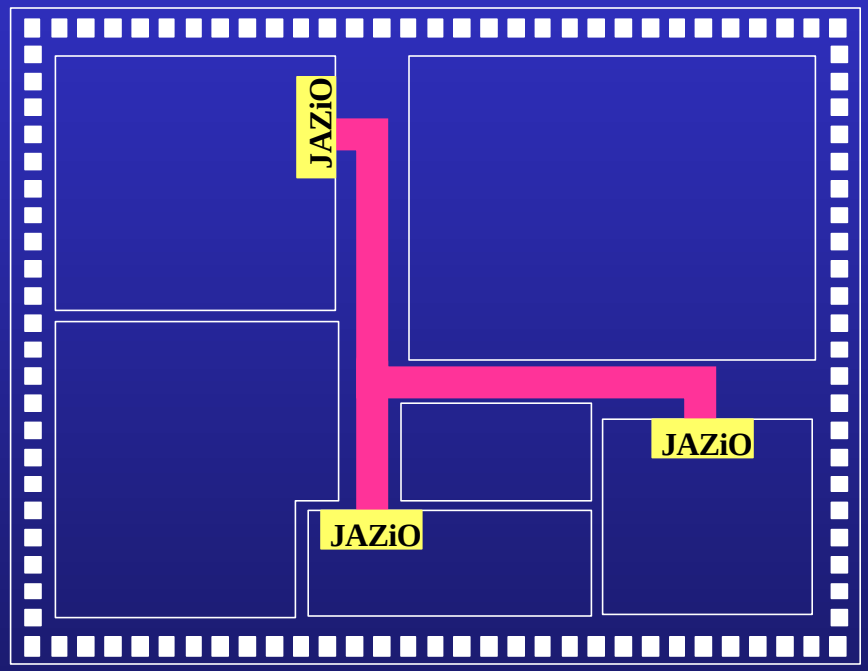
JAZiO makes implementation easier and takes the burden off of meeting set-up time, hold time, and rise/fall times. JAZiO requires no PLL or DLL circuitry to work..

Single cycle power-up initialization allows user to fully utilize standby/sleep mode.

No restriction and full differentiation on bus protocol and definition.

Better performance and scalability compared to GTL+ and HSTL.

Internal Application Example (SOC, Embedded, Etc.)



JAZiO is well suited for large internal bus structures (SOC), which have greater than 2 pf/line loading. JAZiO uses ~0.3V swing with small transmitters and receivers to easily substitute traditional full swing buses. JAZiO also scales as the technology changes (process, voltage, etc.).

JAZiO makes implementation easier and takes the burden off of meeting set-up time, hold time, and rise/fall times. JAZiO requires no PLL or DLL or repeater circuitry to work..

JAZiO can support a variety of bus widths by increasing number of signals lines (pair of VTRs per 18 lines).

JAZiO can support multiple frequencies on a given bus structure, it can be used synchronously or asynchronously, can support multiple supply voltages on the same bus, thus allowing the user flexibility in optimizing any implementation.

What Does JAZiO™ Deliver?

- Sample layout and guidelines for receiver placement, small swing signal isolation and load matching.
- Simulation and netlist with critical conditions.
- Circuit options and testing strategy for signal skews from drivers, board and receiver mismatches.
- Low power option.
- Power-Down mode option.
- Consulting for design, debug and test chip evaluation (100 hours).